

● PRINTER RUSH ●
(PTO ASSISTANCE)

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|---------------------------------|---------------------------------|----------------------------|
| Application : <u>10/760,090</u> | Examiner : <u>Wojciechowicz</u> | GAU : <u>2815</u> |
| From: <u>MR</u> | Location: <u>IDC</u> FMF FDC | Date: <u>10-18-05</u> |
| Tracking #: <u>EPM 10760090</u> | | Week Date: <u>07-04-05</u> |

| DOC CODE | DOC DATE | MISCELLANEOUS |
|---|-----------------|--|
| <input type="checkbox"/> 1449 | _____ | <input type="checkbox"/> Continuing Data |
| <input type="checkbox"/> IDS | _____ | <input type="checkbox"/> Foreign Priority |
| <input checked="" type="checkbox"/> CLM | <u>06-10-05</u> | <input type="checkbox"/> Document Legibility |
| <input type="checkbox"/> IIFW | _____ | <input type="checkbox"/> Fees |
| <input type="checkbox"/> SRFW | _____ | <input type="checkbox"/> Other |
| <input type="checkbox"/> DRW | _____ | |
| <input type="checkbox"/> OATH | _____ | |
| <input type="checkbox"/> 312 | _____ | |
| <input type="checkbox"/> SPEC | _____ | |

[RUSH] MESSAGE: Claim 2 on Clm 06-10-05 ends with
a semi-colon. Claim 2 ends incomplete.

Please resolve.

Thank you,
MR

[XRUSH] RESPONSE: _____

Corrected.

INITIALS: JBH

AMENDMENTS TO THE CLAIMS

Claim 1 (original): In a three terminal silicon based metal insulator semiconductor (MIS) device, the improvement comprising:

a threshold voltage which can be controlled using a first control signal applied to a first terminal of the three terminal silicon based MIS device;

a negative differential resistance (NDR) mode which is enabled when said first control signal exceeds an NDR onset voltage associated with the three terminal silicon based MIS device and said threshold voltage is increased.

Claim 2 (original): The three terminal silicon based MIS device of claim 1, wherein said threshold voltage also is controlled using a second control signal applied to a gate terminal of the three terminal silicon based MIS device/.

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10-21-05

Claim 3 (original): The three terminal silicon based MIS device of claim 1, wherein the device is an n-channel transistor having a polysilicon gate.

Claim 4 (original): The three terminal silicon based MIS device of claim 1, wherein the NDR mode for such device can be disabled through a separate bias voltage applied to a fourth terminal for the device.

Claim 5 (original): The three terminal silicon based MIS device of claim 1, wherein said NDR onset voltage is set during a CMOS compatible manufacturing operation.